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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,977	05/30/2002	Mike Rhoades	8783-US-PA	4066

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
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EXAMINER	
RIZZUTO, KEVIN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/063,977	RHOADES, MIKE	
	Examiner	Art Unit	
	Kevin P Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☒ Claim(s) *2-8 and 11-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 have been examined.

2. Acknowledgement of application filed on 5/30/2002. The papers filed have been placed on record.

Specification

3. The specification is objected to because the title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Collapsible pipeline structure for combining pipeline stages by selectively bypassing storage units."

Claim Objections

4. Claims 2-8, 11, 12 and 13 objected to because of the following informalities:

5. As per claim 2, applicant states "a storage unit, receiving the sequence of instruction stages" when it is believed applicant intended to state instruction stage *results.* Applicant also states, "under controlled by," which is improper English.

6. As per claim 11, applicant claims a "second first storage unit" when there has not been a previous "first storage unit" claimed. "Second first storage unit" lacks antecedent basis.

7. As per claim 12, applicant claims "the collapsible pipeline structure" when there has not been a "collapsible pipeline structure" previously claimed. Applicant also claims "the pipeline stage," in line 4 of claim 12, when there has not been a "pipeline stage" previously claimed. "Collapsible pipeline structure" and "pipeline stage" lack antecedent basis.

8. Claims 3-8 and 13 are objected to because they are dependent on the above claims. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

9. Claims 4, 5, 12 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. As per claim 4, applicant states that "the logic gate unit and the multiplexer of the bypassing storage unit are 'designed together'" and it is unclear what "designed together" means. The specification does not clarify the metes and bounds of this limitation.

11. As per claim 12, applicant states limitations involving the use of the variables "N". Use of the variable "N" renders this claim indefinite since it can be taken to mean negative values, zeros, infinities or fractions. These values, when applied to the number of pipeline stages, present situations that cannot occur. Amend the claim language to more clearly define the metes and bounds of the claimed invention in each instance of the variable "N".

12. Claims 5 and 13 are rejected because they are dependent on the above claims.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 1, 2 and 8-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsuruta, translated Japanese Patent Document No. 01-33351.

15. As per claim 1, a collapsible pipeline structure (Figure 17), suitable for use in a microprocessor, the structure comprising:

-A first pipeline stage (Memory element 63 (not shown) of pipeline stage Pi-1 to the memory element 63 of pipeline stage Pi), under control of a clock to export a sequence of instruction stage results, one result per clock cycle: (Figure 17 shows a pipeline state Pi-1 which is identical to pipeline stage Pi and precedes it, but is drawn without its internal components. It has a clock input that controls the output from Memory element 63 (exporting of instruction stage results)).

-A bypassing storage unit (Memory element 63 and bypass control signal 64), which receives the sequence of instruction stage results from the first pipeline stage (theoretical circuit 61):

-And either captures the sequence in a storage unit with respect to the clock and exports the stored output sequence delayed by one clock cycle, or when operating in collapsed mode, exports the sequence of results from the first stage, directly, bypassing the storage unit: (Page 17 and Figure 17)

-And a second pipeline stage (Memory element 63 of pipeline stage Pi to the memory element 63 (not shown) of pipeline stage Pi+1), which receives the output sequence from the bypassing storage unit (Memory element 63 and bypass control signal 64 of pipeline stage Pi): (Figure 17 shows a pipeline state Pi+1 which is identical to pipeline stage Pi and follows it, but is drawn without its internal components.)

-And exports a sequence of results for the second instruction stage, under control of the clock: (It has a clock input that controls the output from memory element 63 (exporting of instruction stage results)).

-Wherein if the collapsing function of the bypassing storage unit is enabled through the collapse enable signal, then the first and second pipeline stages are collapsed into a single pipeline stage with respect to the clock (Page 17 and 18 and Figure 17)

-Exporting a sequence of collapsed instruction stage results that are the aggregate results of the instruction sequence passing through the first and second pipeline stages, in order: (Page 17 and 18 and Figure 17)

-Wherein if the collapsing function of the bypassing storage unit is disabled through the collapse enable signal, then the instruction stages function in an uncollapsed mode: (Page 17 and 18 and Figure 17)

16. As per claim 2, the collapsible pipeline structure of claim 1, wherein the bypassing storage unit comprises: (Page 17 and 18 and Figures 15 and 17))

-A logic gate unit (Clock control unit 14 of figure 15), receiving the clock and a collapse enable signal (output from the command input control unit 51): (the Clock control unit 14 outputs a clock signal that can be masked, therefore it is inherent that it also receives a clock signal in order for it to be able to control it by masking or not masking it.

-A storage unit (Memory element 63), receiving the sequence of instruction stages from the first pipeline stage (output of theoretical circuit 61: (figure 17)

-And exporting a stored content output under control by a logic output (clock signal) from the logic gate unit (Clock Control unit 14);

-And a multiplexer (Selector 64), receiving the sequence of instruction stage results from the first pipeline stage (from theoretical circuit 61) at a first terminal and the stored result sequence from the storage unit (Memory element 63) at a second terminal. (Figure 17)

-Under control by the collapse enable signal (bypass control signal) to select one of them as an output of the bypassing storage unit (Figure 17)

17. As per claim 8, the collapsible pipeline structure of claim 2, wherein the multiplexer of the bypassing storage unit is a two-to-one multiplexer. (Figure 17

shows the selector unit 64 has two inputs and one output and page 17 explains the multiplexer function of selecting one of the two inputs as an output)

18. As per claim 9, the collapsible pipeline structure of claim 1, wherein the number of the instruction stages being collapsed is two (Figure 17 and pages 17 and 18 in the translation of the specification; When the bypass control signal is set to bypass the memory element and the clock is masked all in the box marked Pi, the said first stage and said second stage are collapsed into one.)

19. As per claim 10, the collapsible pipeline structure of claim 1, wherein the first pipeline stage comprises a first storage unit controlled by the clock and a stage-1 logic circuit coupled in series (Figure 17 and Page 17; All the pipeline stages, Pi-1, Pi, and Pi+1 have the same structure. The memory element 63 of pipeline stage Pi-1 is controlled by a clock and is connected in series to the theoretical circuit 61 of pipeline stage Pi)

20. As per claim 11, the collapsible pipeline structure of claim 1, wherein the second pipeline stage comprises a stage-2 logic circuit (theoretical circuit 62) to receive the output from the bypassing storage unit (Memory element 63), and a second first storage unit (Memory element 63 of pipeline stage Pi+1) coupled in series after the stage-2 logic circuit and controlled by the clock: (Figure 17 and Page 17 of the translation of the specification; All the pipeline stages, Pi-1, Pi, and Pi+1 have the same structure.)

21. As per claim 12, a method for configuring the collapsible pipeline structure in a microprocessor under control of a clock for executing instructions, the method comprising: grouping the pipeline stage (Memory element 63 of pipeline

stage Pi-1 to the memory element 63 of pipeline stage Pi), by selecting N number of consecutive pipeline stages with respect to the instruction flow through the pipeline as a group, for which bypassing storage units (Memory element 63 and selector 64) are employed between each of the N pipeline stages of the group, and for each; collapsing the group as a single stage under control of a clock and with respect to a clock cycle, when the instructions are operated at a low speed least less than or equal to approximately a fraction 1/N times the maximum operation speed of the processor; and selecting one of the pipeline stages in the corresponding group as an output at the desired clock cycle. (Figure 17, pages 17 and 18: Page 18 discusses operating the processor with 2/3 the pipeline stages in bypass mode. Figure 18 shows the only one of every three stages with a clock pulse, thus the frequency is lowered approximately a fraction 1/N times the maximum operating speed of the processor. The one of every three stages that is not in bypass mode is the selected one of the pipeline stages that is an output at the desired clock cycle.

22. As per claim 13, the method of claim 12, wherein the N number is equal to 2. (Figure 17, pages 17 and 18; the number of pipeline stages collapsed in the example given in Tsuruta is three. Therefore, because three collapsed stages contain two collapsed stages, two stages are taught to be collapsed. The approximate fraction of the clock frequency is 1/3 in Tsuruta, which is less than ½.)

23. As per claim 14, a method for configuring a pipeline structure associating an instruction having a plurality of instruction stages under a collapsing operation

mode, the method comprising: partitioning the pipeline stages into a plurality of collapsible stage groups, each one of the collapsible groups including a plurality of the pipeline stages and is treated as a single stage with respect to a clock cycle. (Figure 17, pages 17 and 18)

24. As per claim 15, the method of claim 14, wherein each one of the collapsible stage groups comprises of two pipeline stages. (Figure 17, pages 17 and 18; the number of pipeline stages collapsed in the example given in Tsuruta is three. Therefore, because three collapsed stages contain two collapsed stages, two stages are taught to be collapsed. The approximate fraction of the clock frequency is 1/3 in Tsuruta, which is less than ½.)

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claims 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuruta, Japanese Patent Document No. WO 01-33351.

26. As per claim 3, Tsuruta fails to teach the collapsible pipeline structure of claim 2, wherein the logic gate unit of the bypassing storage unit comprises an AND logic gate. Tsuruta is silent on how the masking of the clock signal is carried out by logic components.

27. The bypass control signal of figure 17 signals to the pipeline stage to be in bypass mode. When it is in bypass mode, the clock for the storage element 63 is masked so as not to operate the storage element 63. Therefore the same function is performed in Tsuruta as in applicant's invention, the clock is masked for the storage unit when the pipeline stage is in bypass mode. The input control unit 51 provides the bypass control signal to the clock controller 14. The clock controller 14 is what masks the clock signal to the storage element. An AND logic gate inside the clock controller 14 would perform this function of masking, because there are two inputs, the clock and the bypass control signal, and an AND logic gate would perform this masking. (Figures 15 and 17, pages 17 and 18).

28. Examiner takes Official Notice that clock masking with an AND logic gate is conventional and well known. An AND logic gate inside the clock controller 14 would perform this function of masking, because there are two inputs, the clock and the bypass control signal, and an AND logic gate would be an obvious logic gate choice because of its simple hardware and well known and conventional logic function it performs.

29. It would have been obvious to one of ordinary skill in the art to use an AND logic gate to perform a masking of the clock since Examiner takes Official Notice that using an AND logic gate to mask a signal is well known and conventional in the art.

30. As per claim 4, Tsuruta teaches wherein the logic gate unit and the multiplexer of the bypassing storage unit are designed together and the

multiplexer receives an original logic state of the collapse enable signal: (Figure 15 and 17, pages 17 and 18; The clock controller 14 which does the masking is shown in figure 15 and it is connected to the pipeline stages by signals and together the multiplexer (selector 64) of the bypassing storage unit and the logic gate unit (clock controller 14) allow the pipeline stages to collapse. Therefore the bypassing storage unit and logic gate unit are designed together. Figure 17 shows that the selector 64 (multiplexer) receives an original logic stage of the bypass control signal (collapse enable signal).

31. Tsuruta fails to teach whereby the logic gate unit receives an inverse logic state of the collapse enable signal. Tsuruta is silent on how the masking of the clock signal is carried out by logic components.

32. The bypass control signal of figure 17 signals to the pipeline stage to be in bypass mode. When it is in bypass mode, the clock for the storage element 63 is masked so as not to operate the storage element 63. Therefore the same function is performed in Tsuruta as in applicant's invention, the clock is masked for the storage unit when the pipeline stage is in bypass mode. The input control unit 51 provides the bypass control signal to the clock controller 14. The clock controller 14 is what masks the clock signal to the storage element. (Figures 15 and 17, pages 17 and 18).

33. Examiner takes Official Notice that clock masking with an AND logic gate with appropriate inputs, such as an inverted signal on one input, is conventional and well known. An AND logic gate inside the clock controller 14 would perform this function of masking, because there are two inputs, the clock and the bypass

control signal, and an AND logic gate would be an obvious logic gate choice because of the well known and conventional logic function it performs. It would have been obvious to invert the Bypass Control Signal as an input to an AND logic gate for clock masking, when an active high signal indicates Bypass Mode, which would be the case when the storage element 63 would have its clock masked in order to keep the storage element idle during that particular clock cycle. With an active high Bypass Control Signal indicates Bypass Mode, an inverted Bypass Control Signal as an input to an AND logic gate would have been a conventional and well known method to mask the clock.

34. It would have been obvious to one of ordinary skill in the art to use an AND logic gate to perform a masking of the clock since it is well known in the art that an AND logic gate is made from simple hardware that can mask one input signal by setting the other input appropriately, which includes using an inverted input to set the signal appropriately to do the masking. (Figures 15 and 17, pages 17 and 18).

35. As per claim 5, the collapsible pipeline structure of claim 4, wherein the logic gate unit comprises an AND logic gate with an inverter at the terminal for receiving the collapse enable signal.

36. Tsuruta fails to teach whereby the logic gate unit comprises an AND logic gate with an inverter at the terminal for receiving the collapse enable signal. Tsuruta in view of the Examiner's Official Notice is silent on how the inverting of the Bypass Control Signal occurs.

37. Examiner takes Official Notice that in order to invert an input signal to a logic component such as an AND logic gate, adding an inverter at the terminal that receives the signal that needs to be inverted is conventional and well known and is simple to design and implement.

38. It would have been obvious to one of ordinary skill in the art at the time of the invention to add an inverter at the terminal that receives the Bypass Control Signal (collapse enable signal) since Examiner takes Official Notice that adding inverters at terminals of logic components such as AND logic gates is well known and conventional.

39. As per claim 6, Tsuruta is silent on whether or not the storage unit of the bypassing storage unit comprises a flip-flop circuit.

40. However, Examiner takes Official Notice that the use of a flip-flop circuit for a storage unit is conventional and well known.

41. It would have been obvious at the time the invention was made to on e of ordinary skill in the art to employ a flip-flop as a storage unit in the device of Tsuruta since Examiner takes Official Notice that the use of a flip-flop as a storage unit is conventional and well known and is easy to design and implement.

42. As per claim 7, Tsuruta is silent on whether or not the storage unit of the bypassing storage unit comprises a latch circuit.

43. However, Examiner takes Official Notice that the use of a latch circuit for a storage unit is conventional and well known.

44. It would have been obvious at the time the invention was made to on e of ordinary skill in the art to employ a latch as a storage unit in the device of Tsuruta since Examiner takes Official Notice that the use of a latch as a storage unit is conventional and well known and is easy to design and implement.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (571) 272-4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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